

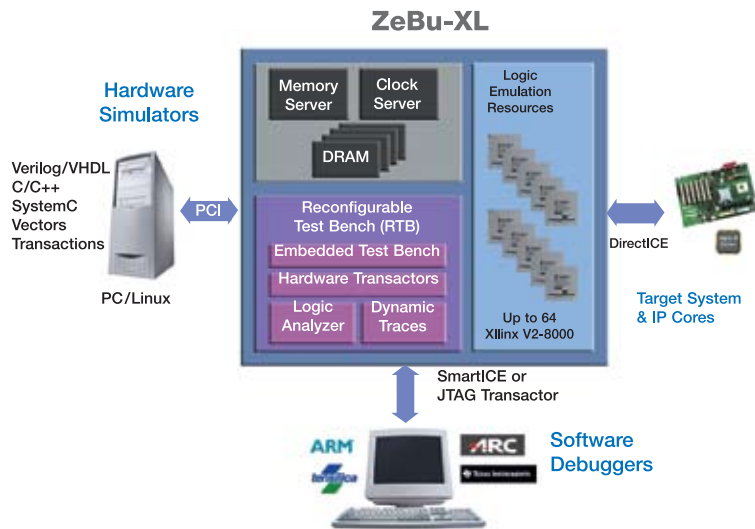


# ZeBu-XL System Emulator

## A New Approach to Verification

EVE has pioneered an entirely new approach to hardware-assisted verification that combines the best aspects of traditional emulation and rapid prototyping systems into a single, unified environment for both ASIC/SoC debugging and embedded software validation.

ZeBu-XL is a high capacity system emulator with the easy setup and debugging associated with emulation, and the price/ performance of rapid prototyping. Configurable to handle designs from 6M to 50M ASIC gates, ZeBu-XL primarily aims at large-scale chip and system emulation applications. It is ideal for the system-integration phase of the design cycle where multiple logic blocks, multiple chips, and embedded software all must be verified together. Hardware design and software development teams can share the same system and design representation, and can easily collaborate when debugging complex hardware/software interactions. The net effect is that hardware/software integration takes place much earlier in the design cycle, thereby reducing silicon respins and accelerating time to market.



ZeBu-XL has been architected for use by both hardware designers and embedded software developers.

ZeBu-XL is offered in a modular, 19 inch rack-mountable configuration, which accepts up to 64 Xilinx Virtex-II XC2V8000 FPGAs. The system has three memory module slots for up to 1.5 GB of embedded memory. ZeBu-XL also features two optional interfaces for connecting the DUT to a software debugger and target system. The software debugger interface, called SmartICE, connects ZeBu-XL to a JTAG port or to any other fast interface with a maximum of 64 I/O pins and 4 clock inputs. The in-circuit emulation interface, called DirectICE, interfaces the emulated design under test to a target system and/or hard IP cores via a maximum of 920 I/O pins and up to 8 clock inputs (or 1840 I/O pins and 16 clock inputs with two DirectICE interfaces).

## ZeBu-XL Application

Leveraging a wide range of operating modes, ZeBu supports hardware verification and embedded software validation throughout the development cycle:

- **Verify and debug ASICs/SoCs, IP cores**  
With its integrated hardware debugging resources and high execution speed, ZeBu is ideal for verifying and debugging complex functional blocks, IP cores and full chip designs. Early in the design cycle ZeBu accelerates simulation in co-emulation with leading HDL simulators and/or C/C++ code or behavioral SystemVerilog testbenches at cycle and transaction level. No changes to existing HDL testbenches are required, and ZeBu also supports HVL testbenches such as Vera™ and e.
- **Co-verify hardware and software integration**  
Later in the design cycle as the pieces of the design come together, ZeBu can validate the entire system by running the embedded software with either a synthesizable test bench or in co-emulation with C++/System C code on the workstation. ZeBu has been architected for especially fast co-emulation at the transaction level, with operating speeds up to 20 MHz.
- **Develop and debug embedded software**  
For software debugging, a JTAG cable or transactor interface connects standard embedded software debuggers from ARM, TI, ARC, Tensilica, etc, to the SoC under development. In this way ZeBu can execute software drivers, operating systems or applications at MHz speed, while providing full hardware and software debugging capabilities to both hardware and software engineers on the same design representation. For pure software debugging applications EVE offers a "replicate" version of ZeBu that is optimized for the needs of embedded software developers, at a fraction of the cost of a full ZeBu system.



THE FASTEST VERIFICATION



ZeBu-XL is housed in a 19" rack mountable chassis

## Key Features for Hardware Verification

### Rapid setup with the ZeBu Compiler:

- Completely automated compiler from RTL to the emulator binary files, including:
  - Memory generation & pre-defined memory models
  - Automatic clock-tree mapping to remove timing violations due to gatedclocks/muxed-clocks/divided clocks
  - Automatic clustering of netlist into array of FPGA's
  - Fast, parallel synthesis and P&R on multiple PCs
  - Incremental compilation for quick design turn-around

### Comprehensive hardware debugging environment, including:

- Run-time read/write access of all registers & memories
- Complete internal state capture without re-compilation
- I/O pin & static probe tracing via on-board trace memory
- H/W Triggers to trace-on-trigger and stop-on-trigger
- VCD & FSDB generation & Waveform API
- Save/restore

### Integration with popular hardware design tools:

- Co-emulation with HDL Simulators: VCS™, NC-Sim™, ModelSim™

## Key Features for HW/SW Co-verification and Embedded SW Validation

- High speed operation for fast execution of large software programs
- Interfaces to popular embedded software debuggers for ARM, ARC, Tensilica, TI, and other CPU/DSP cores via:
  - SmartICE interface or
  - JTAG transactor
- Interface to ARM Logic Tiles via the DirectICE interface
- Save/restore function to bypass lengthy boot sequences when recreating problems
- Enables hardware designers and software developers to collaborate on a common design representation for quickest resolution of HW/SW integration issues
- Available in reduced-cost "replicate" configuration for embedded software development

Emulation Operating Modes	Performance Range
Co-emulation with commercial HDL simulator	5K - 100KHz
Co-emulation with signal-level C/C++/SystemC	100K - 500KHz
Co-Emulation with transaction-level C/C++/SystemsC/SystemVerilog	200K - 10MHz
Test vectors	100K - 500KHz
Emulation with synthesizable test bench	±10MHz
In-circuit emulation, connected to target system	±10MHz
Emulation with SW debuggers via JTAG interface	±10MHz

ZeBu's operating modes and the corresponding operating performance

ZeBu-XL Product Specifications and System Requirements	
Logic capacity	6M-50M ASIC gates
On-board RAM	Up to 1.5GB
Operating performance	Up to 10MHz (see Operating Mode table)
DirectICE interface	920 unmultiplexed I/O pins + 8 clock inputs – up to two DirectICE interfaces
SmartICE interface	64 I/O pins + 4 clock
System interface supported	DRAM, FLASH, LCD, DTV, UART, JTAG, PCIe, Ethernet, and others
Dynamic probe capacity	Run-time access to all registers and memories
Form factor	19" rack mountable chassis
PCI Interface	64bit x 66MHz
OS	Linux RH 8.0, Linux RH Enterprise 3, Suse Enterprise 9.0
Recommended host PC	PC Pentium class, 3GHz, 1GB RAM
Board dimensions [cm/in]	(69x27x45) / (27"x10.5"x17.5")
Power Consumption	110V or 220V - 15A



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